

WHAT IS CLAIMED IS:

1. A clock generator for providing programmable control of an output clock, the clock generator comprising:
 - (a) a mechanism for creating a plurality of clocks offset in phase;
 - (b) two programmable selectors for selecting two clocks from the plurality of clocks; and
 - (c) logic for combining the two selected clocks to create an output clock with any combination of offset, if any, and width.
2. The clock generator as in claim 1 further comprising a logic element for starting and stopping the output clock.
3. The clock generator as in claim 1 further comprising a logic element for starting and stopping the two selected clocks from the programmable selectors.
4. The clock generator as in claim 1 further comprising a logic element for starting and stopping the plurality of clocks.
5. The clock generator as in claim 1, wherein the mechanism for creating the plurality of clocks includes a delay lock loop.
6. The clock generator as in claim 1, wherein the mechanism for creating the plurality of clocks includes a programmable clock generator and at least one shift register.
7. A clock generator for providing programmable control of an output clock, the clock generator comprising:
 - (a) a mechanism for creating a plurality of clocks offset in phase;
 - (b) a programmable selector for selecting a clock from the plurality of clocks; and

(c) logic for controlling the selected clock to create an output clock with any offset.

8. The clock generator as in claim 7 further comprising a logic element for starting and stopping the plurality of clocks.

9. The clock generator as in claim 7, wherein the mechanism for creating the plurality of clocks includes a delay lock loop.

10. The clock generator as in claim 7, wherein the mechanism for creating the plurality of clocks includes a programmable clock generator and at least one shift register.